

CLAIMS

What is claimed is:

- 1 1. A processor, comprising:
2 a decoder to implement a first and second flow synonym for a first
3 instruction, said decoder to associate one of said first and second flow
4 synonym with said first instruction; and
5 a scheduler to schedule said one of said first and second flow
6 synonym for execution.
- 1 2. The processor of claim 1, wherein said first flow synonym is
2 to execute on a first execution unit and said second flow synonym is to
3 execute on a second execution unit.
- 1 3. The processor of claim 2, wherein said first execution unit
2 and said second execution unit are of differing types.
- 1 4. The processor of claim 2, wherein said first execution unit
2 and said second execution unit are of differing precisions.
- 1 5. The processor of claim 1, wherein said first flow synonym
2 and said second flow synonym are to execute on a common execution
3 unit.
- 1 6. The processor of claim 1, wherein said decoder is to make
2 said association based upon processor status.

1 7. The processor of claim 1, wherein said decoder is to make
2 said association based upon a rule.

1 8. The processor of claim 7, wherein said rule considers a
2 power configuration of said processor.

1 9. The processor of claim 7, wherein said rule considers
2 failure status of an execution unit.

1 10. The processor of claim 1, wherein said decoder is further to
2 associate other one of said first and second flow synonym with said first
3 instruction, and wherein said scheduler is further to schedule said
4 other one of said first and second flow synonym for execution.

1 11. The processor of claim 10, further comprising a retirement
2 module to retire whichever said first or said second flow synonym first
3 completes execution.

1 12. The processor of claim 10, further comprising a retirement
2 module to compare execution results of said first and said second flow
3 synonym and raise an exception upon mismatch.

1 13. A method, comprising: ~
2 determining whether each of a plurality of execution units is
3 available; and
4 if a first one of said plurality of execution units is available, then
5 choosing a first flow synonym corresponding to said first available
6 execution unit and further scheduling said first flow synonym for
7 execution on said first available execution unit.

1 14. The method of claim 13, further comprising if none of said
2 plurality of execution units is available, then arbitrating to select a
3 second flow synonym from a plurality of flow synonyms.

1 15. The method of claim 13, further comprising if more than
2 one of said plurality of execution units is available, then choosing said
3 first flow synonym from a plurality of flow synonyms corresponding to
4 one of said available execution units based upon system performance
5 rules.

1 16. The method of claim 13, wherein said determining includes
2 reading a processor status register.

1 17. The method of claim 16, wherein said processor status
2 register indicates a second one of said execution units is less available
3 due to a fault in said second one of said execution units.

1 18. The method of claim 16, wherein said processor status
2 register indicates a second one of said execution units is available due
3 to a processor reduced power mode.

1 19. A method, comprising:

2 decoding an instruction into a first flow synonym and a second

3 flow synonym;

4 scheduling said first flow synonym and said second flow synonym

5 for execution on a first execution unit and a second execution unit;

6 executing said first flow synonym on said first execution unit; and

7 executing said second flow synonym on said second execution

8 unit.

1 20. The method of claim 19, further comprising retiring said
2 first flow synonym when said first flow synonym finishes execution
3 before said second flow synonym finishes execution.

21. The system of claim 19, further comprising raising an exception when a first execution result of said first flow synonym does not equal a second execution result of said second flow synonym.

1 22. A system, comprising: 4
2 a processor including a decoder to implement a first and second
3 flow synonym for a first instruction, said decoder to associate one of
4 said first and second flow synonym with said first instruction, and a
5 scheduler to schedule said one of said first and second flow synonym
6 for execution;
7 an interface to couple said processor to input/output circuitry;
8 and
9 an audio input/output circuitry coupled to said interface.

1 23. The system of claim 22, wherein said first flow synonym is
2 to execute on a first execution unit and said second flow synonym is to
3 execute on a second execution unit.

1 24. The system of claim 23, wherein said first execution unit
2 and said second execution unit are of differing types.

1 25. The system of claim 23, wherein said first execution unit
2 and said second execution unit are of differing precisions.

1 26. The system of claim 22, wherein said first flow synonym
2 and said second flow synonym are to execute on a common execution
3 unit.

1 27. The system of claim 22, wherein said decoder is to make
2 said association based upon processor status.

1 28. The system of claim 22, wherein said decoder is to make
2 said association based upon a rule.

1 29. The system of claim 28, wherein said rule considers a
2 power configuration of said processor.

1 30. The system of claim 28, wherein said rule considers failure
2 status of an execution unit.

1 31. The system of claim 22, wherein said decoder is further to
2 associate other one of said first and second flow synonym with said first
3 instruction, and wherein said scheduler is further to schedule said
4 other one of said first and second flow synonym for execution.

1 32. The system of claim 31, further comprising a retirement
2 module to retire whichever said first or said second flow synonym first
3 completes execution.

1 33. The system of claim 31, further comprising a retirement
2 module to compare execution results of said first and said second flow
3 synonym and raise an exception upon mismatch.

1 34. A processor, comprising:
2 means for determining whether each of a plurality of execution
3 units is available; and
4 if said means for determining determines that a first one of said
5 plurality of execution units is available, then means for choosing a first
6 flow synonym corresponding to said first available execution unit and
7 further means for scheduling said first flow synonym for execution on
8 said first available execution unit.

1 35. The processor of claim 34, further comprising if said means
2 for determining determines that none of said plurality of execution units
3 is available, then means for arbitrating to select a second flow synonym
4 from a plurality of flow synonyms.

1 36. The processor of claim 34, further comprising if said means
2 for determining determines that more than one of said plurality of
3 execution units is available, then means for choosing said first flow
4 synonym from a plurality of flow synonyms corresponding to one of said
5 available execution units based upon system performance rules.

1 37. The processor of claim 34, wherein said means for
2 determining includes means for reading a processor status register.

1 38. The processor of claim 37, wherein said processor status
2 register indicates a second one of said execution units is less available
3 due to a fault in said second one of said execution units.

1 39. The processor of claim 37, wherein said processor status
2 register indicates a second one of said execution units is available due
3 to a processor reduced power mode.

1 40. A processor, comprising:
2 means for decoding an instruction into a first flow synonym and a
3 second flow synonym;
4 means for scheduling said first flow synonym and said second
5 flow synonym for execution on a first execution unit and a second
6 execution unit;
7 means for executing said first flow synonym on said first
8 execution unit; and
9 means for executing said second flow synonym on said second
10 execution unit.

1 41. The processor of claim 40, further comprising means for
2 retiring said first flow synonym when said first flow synonym finishes
3 execution before said second flow synonym finishes execution.

1 42. The processor of claim 40, further comprising means for
2 raising an exception when a first execution result of said first flow
3 synonym does not equal a second execution result of said second flow
4 synonym.